Amendments to the Drawings:

The attached replacement sheets of drawings includes changes to Fig. 1, 2-1, 2-2 and 3, and replace the original sheets including Fig. 1, 2-1, 2-2 and 3.

In Figure 1, applicant removed the reference numerals 13a and 13b.

In Figure 2-1, applicant changed the reference numeral 14, pointing to the multithreaded processor shown in the figure, to reference numeral 12. Applicant further removed reference numeral 56 which was pointing to the element block identified as "PLL GRAMMAR."

In Figure 2-2, applicant changed the reference numeral 29, pointing to the element block identified as the Scratch Pad, to reference numeral 27. Applicant also removed the reference numerals 29a, 29b, and 29c. Further, applicant replaced "SDRAM" with "SRAM" in element block 16b.

In Figure 3, the applicant marked the element identified as uPC_1 with reference numeral 72a (which previously pointed to uPC_4), uPC_2 with reference numeral 72b (which previously pointed to uPC-1), and uPC_3 with reference numeral 72c (which previously pointed to the illustrated multiplexer). Additionally, applicant added new reference numeral 72d to mark uPC_4.

Attachments following last page of this Amendment:

Replacement Sheet (4 pages)
Annotated Sheet Showing Change(s) (4 pages)

REMARKS

Claims 1-25 are pending. Claims 1, 11 and 21 are independent.

Applicant canceled without prejudice claims 8 and 18.

The examiner objected to the drawings under various grounds. Applicant amended FIGS. 1, 2-1, 2-2 and 3 in accordance with the examiner's comments.

The examiner indicated that that an unrecognizable character appears in front of the term "CUS" in the first paragraph of page 2 of the Specification. Applicant replaced "□CUS" with "μCUS" to correct the typographical error identified by the examiner.

The examiner requested that the title of the application be changed. Applicant amended the title in accordance with the examiner's suggestion.

The examiner rejected claims 1-10 under 35 U.S.C. §101 on the ground that the claims are directed to a non-statutory subject- matter. Applicant amended claims 1-7 and 9-10 to recite in the pre-amble "a computer program product residing on a computer readable storage medium comprising instructions, including a branch instruction that when executed on a computing device causes the computing device to: ... ." With these amendments to the pre-amble of claims 1-7, 9-10, applicant submits that the claims are directed to statutory subject matter, namely a computer readable storage medium which is an article of manufactures.

The examiner objected to claims 4-5 and 7-9 on the ground that the claims appear to be method claims even though claim 1, from which the claims depend, appears to be directed to an apparatus. As noted above, independent claim 1 and its dependent claims have been amended so as to be directed to a computer program product claim that includes a branch instruction. Claims 4-5, 7 and 9 (claim 8 has been cancelled) recite features pertaining to tokens of the branch instruction that is part of the claimed computer program product of claims 1-7 and 9-10. Applicant submits that claims 1-7 and 9-10, including claims 4-5, 7 and 9, all recite subject matter directed to computer program products, and as such the subject matter of claims 4-5, 7 and 9 is properly claimed.

The examiner rejected claims 4-5 and 7-8 under 35 U.S.C. §112, second paragraph, on the ground that it is not clear whether the optional token recited in those claims is an essential part of the invention or not.

Applicant respectfully disagrees with the examiner's contentions.

Firstly, applicant submits that the alleged recitation of non-essential subject matter is not a proper ground for rejection. As explained in MPEP 2172.01:

> **Ex parte Nolden, 149 USPQ 378, 380 (Bd. Pat. App. 1965) ("[I]t is not essential to a patentable combination that there be interdependency between the elements of the claimed device or that all the elements operate concurrently toward the desired result"); Ex parte Huber, 148 USPQ 447, 448-49 (Bd. Pat. App. 1965) (A claim does not necessarily fail to comply with 35 U.S.C. 112, second paragraph where the various elements do not function simultaneously, are not directly functionally related, do not directly intercooperate, and/or serve independent purposes.)**

Furthermore, applicant notes that in any event claims 4-5 and 7 (claim 8 has been cancelled) are all directed to tokens of a branch instruction that is part of the computer program product of claims 1-7 and 9-10 (see also page 13, line 13, to page 14, line 8, of the Specification). As such, the optional tokens recited in claims 4-5 and 7 are germane to the branch instruction recited in claims 1-7 and 9-10.

The examiner rejected claims 1-25 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 3,577,189 to Cocke et al.

Applicant amended independent claim 1 to make it more clear that the register and the bit of that register upon which the branching decision is based are specified in the branch instruction recited in the claim. Support for this clarification is provided at page 13, lines 13-19, of the Specification. Applicant similarly amended independent claims 11 and 21.

In addition, applicant amended the preamble of claims 2-5, 7 and 23 to recite "wherein the branch instruction comprises." Applicant amended claims 9-10 to clarify that the recited instruction is the branch instruction. Applicant also amended claim 13 to replace "an instruction" with "another instruction" for greater clarity. Further, applicant amended claim 25 to recite "the one of the registers" instead of "the register" for greater clarity.

Cocke describes an apparatus and method for an improved program branching from a first instruction sequence to a second instruction sequence (Abstract). Cocke explains:

> **With reference to FIG. 4A, there is seen a representation of an instruction which may be used in the present invention. As seen in that FIG., the instruction comprises an OP code field, and I-, J-, K-, and H-fields. The OP code of the instruction designates the operation which the instruction signifies. For example, if an OP code is eight binary bits wide, there is a possibility of 256 operations which that field can signify. In the present example, branch instructions comprise a subset of the group of possible OP code configurations. For example, eight types of branch instructions can be signified, each signifying a branch on a different machine condition. The condition is generally determined by a function of two bits of a condition register, explained subsequently. It is recognized that more than two bits can be used in the conditioned determination if desired. The I- and J- fields of the instructions select the two bits of the condition register. (Cocke, col. 4, lines 49-64).**

With respect to the condition register, Cocke further explains:

> **Condition register 56 is seen in detail in FIG. 3. This register comprises a plurality of flip-flops, here shown illustratively as 32 in number, and designated C0, C1, C2,..., C31. Two pairs of output lines 58, 60 are provided as output from the register. ... the I-field and the J-field [of the OP branch code] will indicate one out of the 32 bits of the C-register upon which the function will be computed in the function generator 62 to determine whether or not the branch condition designated by a branch instruction in Row 0 is successful. (col. 6, line 70, to col. 7, line 16)**

Thus, while Cocke discloses branch instructions that specify bit locations of the condition register, Cocke's branch instructions do not specify a selected register because the register used for evaluating branch conditions is always the condition register. Therefore, Cocke's branch instructions have no need to specify the register with respect to which the branching condition will be evaluated and thus Cocke neither discloses nor suggests at least the feature of "cause an instruction stream to branch to another instruction in the instruction stream based on a bit of a specified register being set or cleared, the branch instruction specifying which bit of the specified register to use as a branch control bit," as required by applicant's independent claim 1.

The examiner referred to Cocke's column 10, lines 24-31, as disclosing the features of applicant's independent claim 1. The above-identified excerpt from Cocke states as follows:

> **The activation of line 109 is a signal to the storage system which causes the target instruction bit in the target instruction contained at the effective**

> **branch address to be set to a one so that it can be identified as the target instruction when it reaches the buffer 2. This can be done in the storage system by any well-known means, such as using line 109 as a setting signal for a bit position in the register in the storage system from which the instruction proceeds to bus 1 of FIG. 1A.**

Cocke also explains, at col. 5, lines 20-26, that:

> **As seen in FIG. 1A, instructions enter via gate 4 at A-time from the storage system and proceed over bus 6. The entire instruction, including a bit indicative of the fact that a given instruction is the target instruction, that is, the instruction from the effective branch address to which a program is to branch, is entered into buffer 2.**

Thus, in the above passage identified by the examiner, Cocke merely describes that a bit of a branch target instruction is set to enable identification of that instruction when a branching operation is performed. But that instruction, with respect to which the bit is set, is not itself a branch instruction (unless branching from a branch instruction happens to be to another branch instruction), and in any event, that instruction does not specify a register and a bit, the content of which is used to determine whether or not the branching operation is to be performed.

Thus, Cocke does not disclose or suggest at least "a branch instruction that when executed on a computing device causes the computing device to: cause an instruction stream to branch to another instruction in the instruction stream based on a bit of a specified register being set or cleared, the branch instruction specifying which bit of the specified register to use as a branch control bit," as require by applicant's independent claim 1. Applicant's independent claim 1 is therefore patentable over the cited art.

Claims 2-7 and 9-10 depend from independent claim 1 and are therefore patentable for at least the same reasons as independent claim 1.

Applicant's independent claims 11 and 21 recite "evaluating a bit of a register designated to use as a branch control bit, the bit and the register being specified in a branch instruction; and performing a branching operation based on the specified bit of the specified register being set or cleared," or similar language. For reasons similar to those provided with respect to independent claim 1, at least these features are not discloses by the cited art. Accordingly, applicant's independent claims 11 and 21 are patentable over the cited art.

Claims 12-17 and 19-20 depend from independent claim 11, and are therefore patentable for at least the same reasons as independent claim 11.

Claims 22-25 depend from independent claim 21 and are therefore patentable for at least the same reasons as independent claim 21.

It is believed that all the rejections and/or objections raised by the examiner have been addressed.

In view of the foregoing, applicant respectfully submits that the application is in condition for allowance and such action is respectfully requested at the examiner's earliest convenience.

All of the dependent claims are patentable for at least the reasons for which the claims on which they depend are patentable.

Canceled claims, if any, have been canceled without prejudice or disclaimer.

Any circumstance in which the applicant has (a) addressed certain comments of the examiner does not mean that the applicant concedes other comments of the examiner, (b) made arguments for the patentability of some claims does not mean that there are not other good reasons for patentability of those claims and other claims, or (c) amended or canceled a claim does not mean that the applicant concedes any of the examiner's positions with respect to that claim or other claims.

Please apply any charges or credits to deposit account 06-1050, referencing attorney docket No. 10559-304US1.

Respectfully submitted,

Date: Sept 22, 2006

Ido Rabinovitch
Reg. No. L0080

Fish & Richardson P.C.
225 Franklin Street
Boston, MA 02110
Telephone: (617) 542-5070
Facsimile: (617) 542-8906